

Matched N-Channel JFET Pairs

Product Summary

Part Number	V _{GS(off)} (V)	V _{(BR)GSS} Min (V)	g _{fs} Min (mS)	I _G Typ (pA)	V _{GS1} - V _{GS2} Max (mV)
2N5911	-1 to -5	-25	5	-1	10
2N5912	-1 to -5	-25	5	-1	15

2N5912, For applications information see AN102, page 6.

Features

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 85 dB

Benefits

- Minimum Parasitics Ensuring Maximum High-Frequency Performance
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

Applications

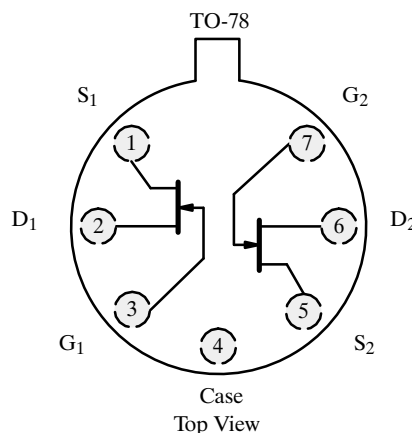
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

Description

The 2N5911/5912 are matched pairs of JFETs mounted in a TO-78 package. This two-chip design reduces parasitics and gives better performance at high frequencies while ensuring extremely tight matching.

For similar products see the SO-8 packaged SST440/SST441, the TO-71 packaged U440/U441, the low-noise SST/U401 series, and the low-leakage U421/423 data sheets.

The hermetically-sealed TO-78 package is available with full military screening per MIL-S-19500 (see Military Information).



Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage	-25 V
Gate-Gate Voltage	±80 V
Gate Current	50 mA
Lead Temperature (1/16" from case for 10 sec.)	300°C
Storage Temperature	-65 to 200°C
Operating Junction Temperature	-55 to 150°C

Power Dissipation :	Per Side ^a	367 mW
	Total ^b	500 mW

Notes

- Derate 3 mW/°C above 25°C
- Derate 4 mW/°C above 25°C

Specifications^a

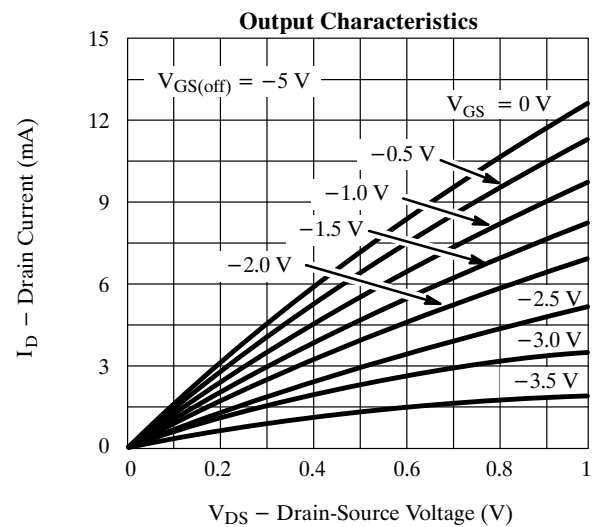
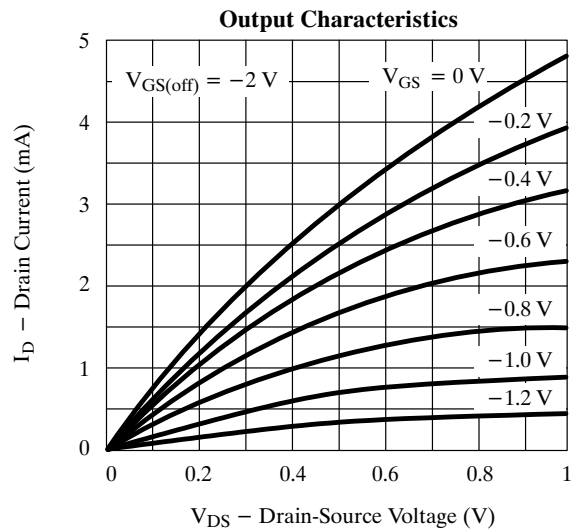
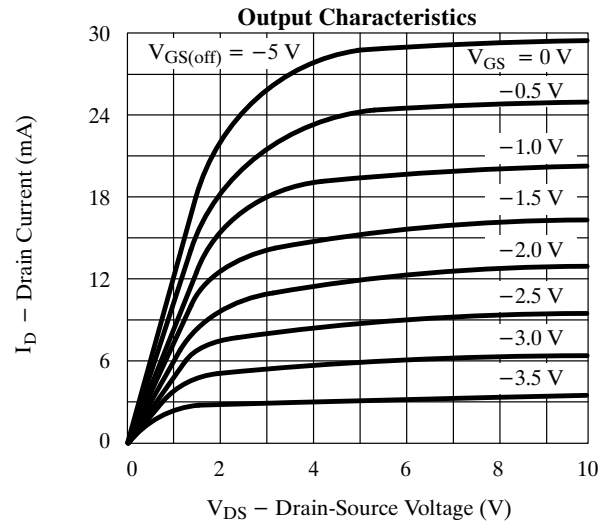
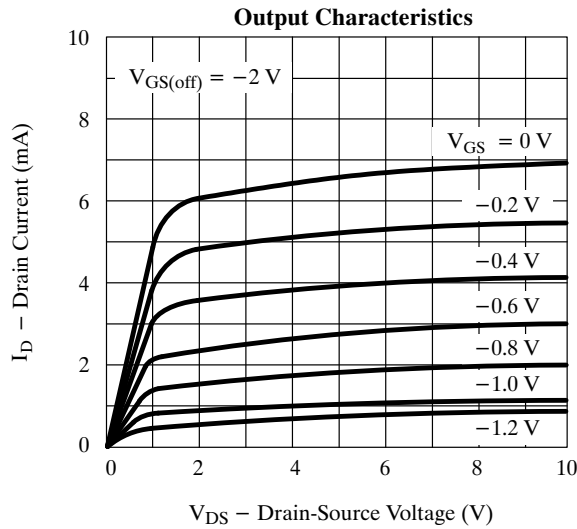
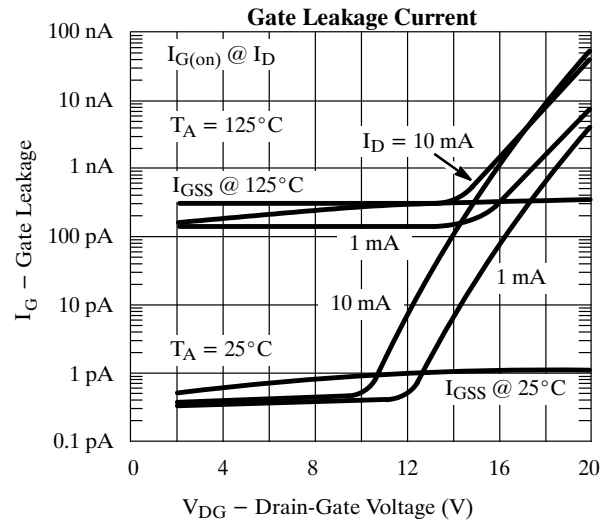
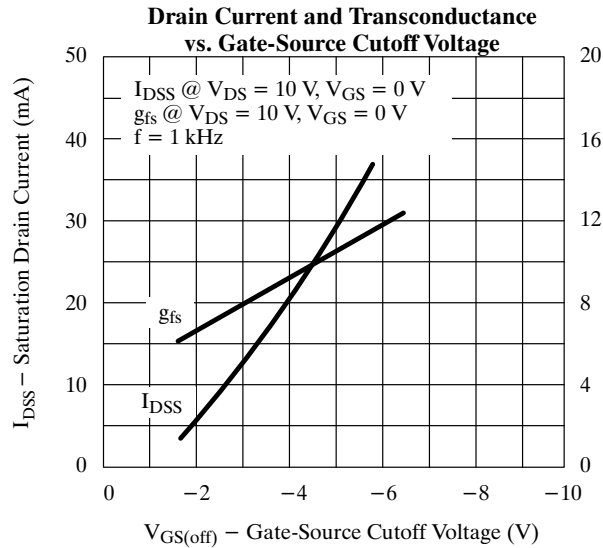
Parameter	Symbol	Test Conditions	Typ ^b	Limits				Unit
				2N5911		2N5912		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 10 V, I_D = 1 nA$	-3.5	-1	-5	-1	-5	
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 10 V, V_{GS} = 0 V$	15	7	40	7	40	mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -15 V, V_{DS} = 0 V$	-1		-100		-100	pA
		$T_A = 150^\circ C$	-2		-250		-250	nA
Gate Operating Current	I_G	$V_{DG} = 10 V, I_D = 5 mA$	-1		-100		-100	pA
		$T_A = 125^\circ C$	-0.3		-100		-100	nA
Gate-Source Voltage	V_{GS}	$V_{DG} = 10 V, I_G = 5 mA$	-1.5	-0.3	-4	-0.3	-4	V
Gate-Source Forward Voltage ^d	$V_{GS(F)}$	$I_G = 1 mA, V_{DS} = 0 V$	0.7					V
Dynamic								
Common-Source Forward Transconductance	g_{fs}	$V_{DG} = 10 V, I_D = 5 mA$ $f = 1 kHz$	6	5	10	5	10	mS
Common-Source Output Conductance	g_{os}		70		100		100	μS
Common-Source Forward Transconductance	g_{fs}	$V_{DG} = 10 V, I_D = 5 mA$ $f = 100 MHz$	5.8	5	10	5	10	mS
Common-Source Output Conductance	g_{os}		90		150		150	μS
Common-Source Input Capacitance	C_{iss}	$V_{DG} = 10 V, I_D = 5 mA$ $f = 1 MHz$	3		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		1.2		1.2	
Equivalent Input Noise Voltage	\bar{e}_n	$V_{DG} = 10 V, I_D = 5 mA$ $f = 10 kHz$	4		20		20	nV/ \sqrt{Hz}
Noise Figure	NF	$R_G = 100 k\Omega$	0.1		1		1	dB
Matching								
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$V_{DG} = 10 V, I_D = 5 mA$	4		10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	$V_{DG} = 10 V, I_D = 5 mA$ $T_A = -55 \text{ to } 125^\circ C$	15		20		40	$\mu V/^\circ C$
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	$V_{DS} = 10 V, V_{GS} = 0 V$	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	$V_{DS} = 10 V, I_D = 5 mA$ $f = 1 kHz$	0.98	0.95	1	0.95	1	
Differential Gate Current	$ I_{G1} - I_{G2} $	$V_{DG} = 10 V, I_D = 5 mA, T_A = 125^\circ C$	0.005		20		20	nA
Common Mode Rejection Ratio ^d	CMRR	$V_{DG} = 5 \text{ to } 10 V, I_D = 5 mA$	85					dB

Notes

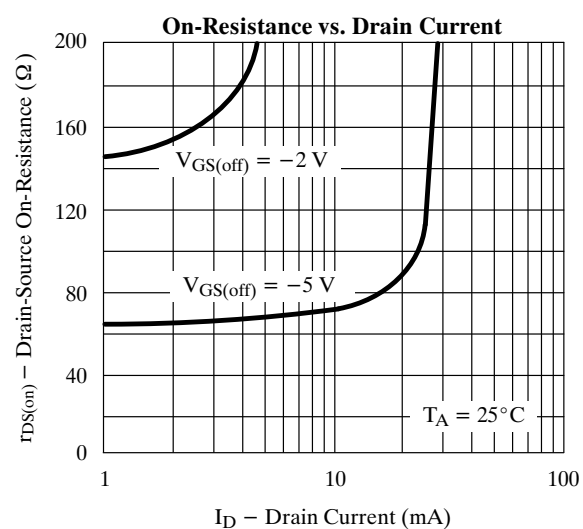
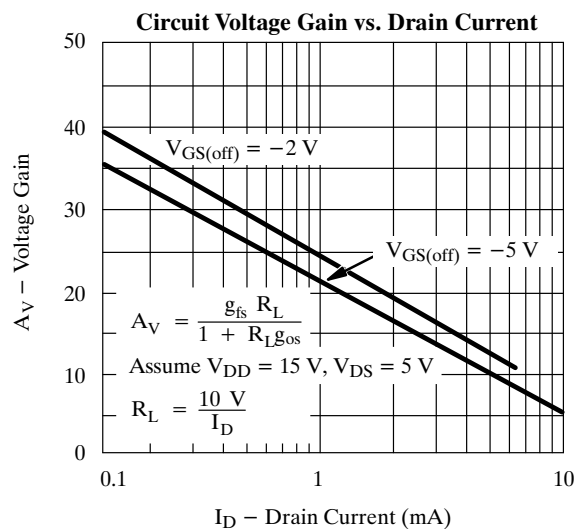
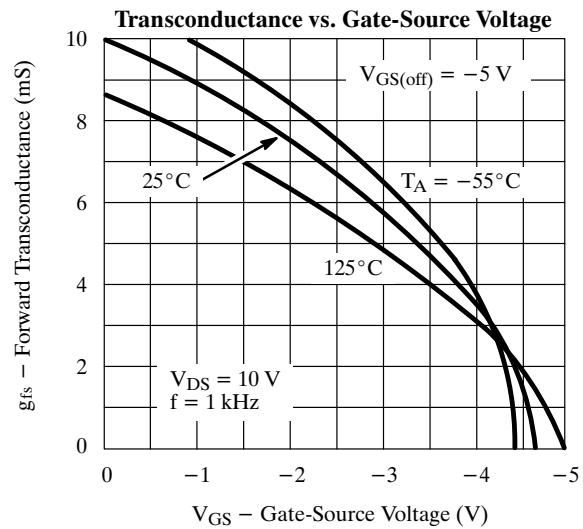
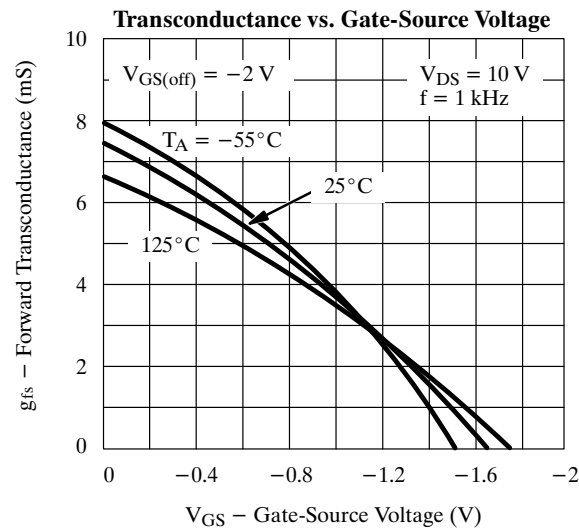
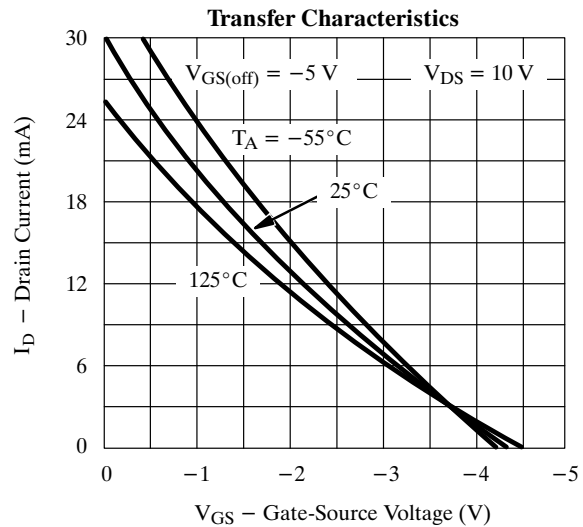
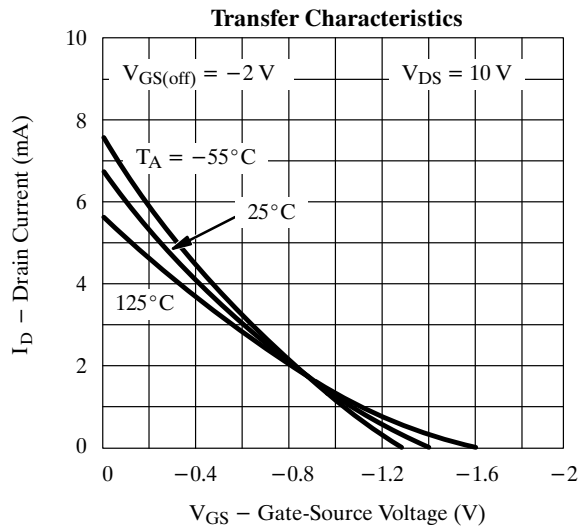
- a. $T_A = 25^\circ C$ unless otherwise noted.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 3\%$.
d. This parameter not registered with JEDEC.

NZF

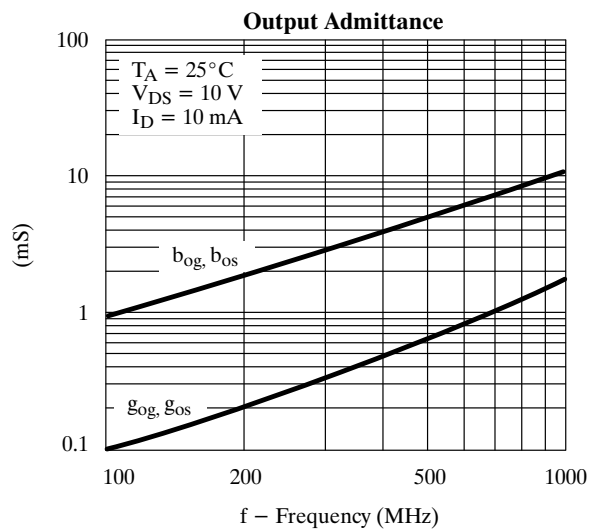
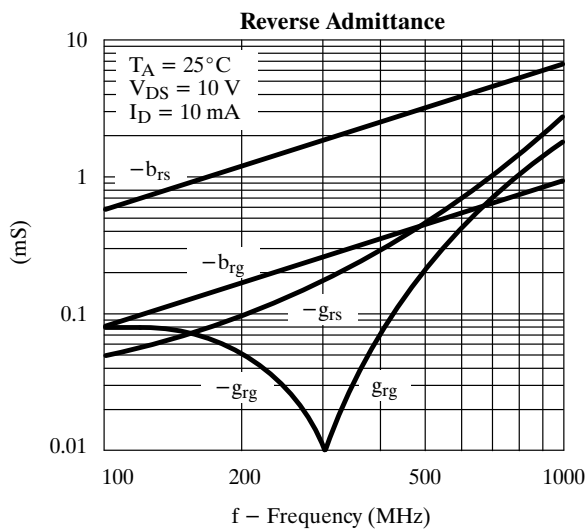
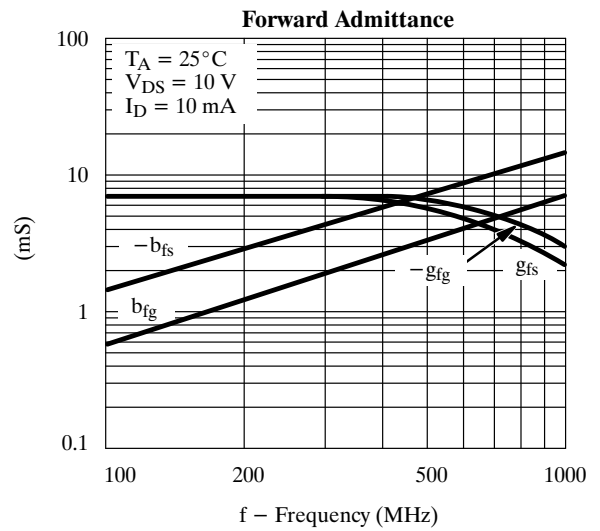
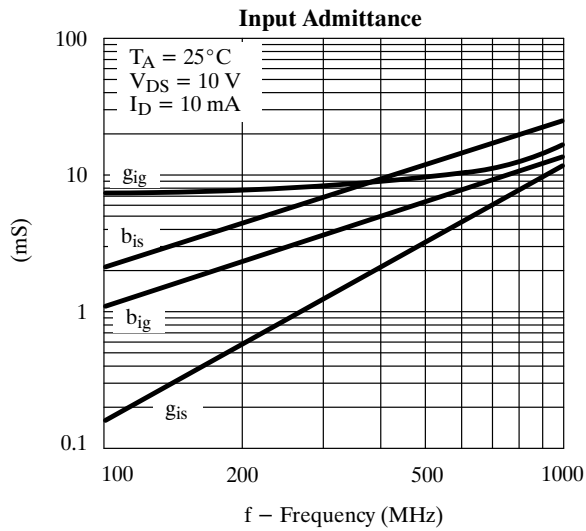
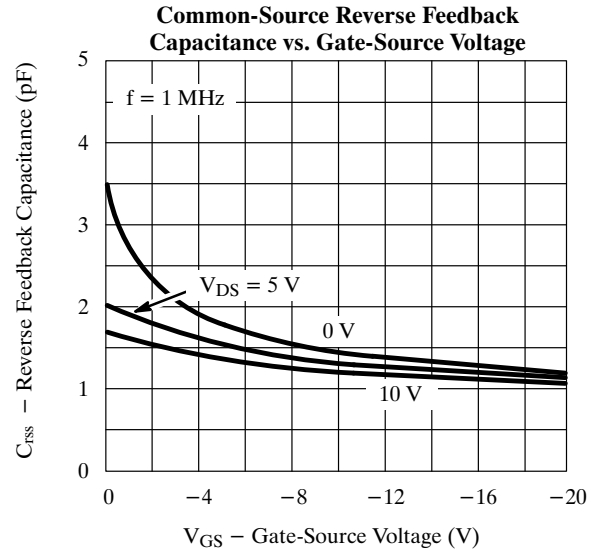
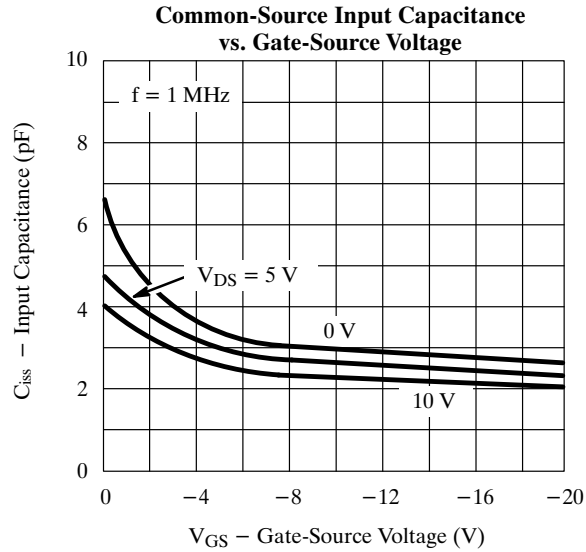
Typical Characteristics



Typical Characteristics (Cont'd)



Typical Characteristics (Cont'd)



Typical Characteristics (Cont'd)

